Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 1. (Currently amended): A method for reading data from a synchronous memory of the type having data cells arranged in rows and columns and having a single row 2 3 cache, comprising: 4 arranging said synchronous memory in a symmetrical layout to include a left 5 plurality of N memory portions including a left memory block, a central sense amplifier block, 6 and a right memory block; a centrally located single row cache; and a right plurality of N 7 memory portions including a left memory block, a central sense amplifier block, and a right memory block, wherein N is at least equal to two; 8 9 receiving an initial command and row address data for reading contents of a row 10 of said synchronous memory selected by said row address data, said reading being performed 11 exclusive of column address data; 12 moving said contents of said row into said single row cache; 13 after said contents of said row have been moved into said single row cache, receiving a "read" command and column address data; and 14 15 in response to said "read" command, reading data from said single row cache at a 16 column address specified by said column address data for output by said synchronous memory. 2. 1 (Original): The method of claim 1 wherein said initial command is 2 received substantially concurrently with said row address data. (Original): The method of claim 1 wherein said "read" command and said 1 3. 2 column address data are received substantially concurrently.

l	4.	(Previously presented): The method of claim 1 further comprising moving
2	said data read from s	aid single row cache to an output of said synchronous memory after a
3	predetermined numb	er of clock cycles after said "read" command.
ł	5.	(Previously presented): The method of claim 4 wherein moving said data
)		ache to an output of said synchronous memory after a predetermined
- 2		es comprises moving said data read from said single row cache to an output
, 1	of said memory after	
•	of said memory after	two clock cycles.
l	6.	(Original): The method of claim 4 wherein said predetermined number of
2	clock cycles is two.	
l	7.	(Original): The method of claim 1 wherein said receiving an initial
2	command comprises	receiving a "bank activate" command.
l	8.	(Original): The method of claim 1 further comprising performing a first
2	precharging operation	n prior to receiving said initial command.
l	9.	(Previously presented): The method of claim 4 further comprising
2	initiating a memory of	operation after said contents of said row have been moved into said single
3	row cache and before	said data read from said single row cache has been moved to said output of
1	said synchronous me	mory.
l	10.	(Currently amended): The method of claim 9 wherein said memory
2	operation is comprise	es a precharging operation.
Į	11.	(Currently amended): The method of claim 9 wherein said synchronous
)	memory is comprises	•
-	mondy to comprise	

12-27. (Canceled)

1	28. (New): A synchronous memory comprising:
2	a plurality of first memory blocks;
3	a first row decoder to access a row of data in the first memory blocks in response
4	to a row address;
5	a row cache configured to receive and to store therein an entire row of data from
6	the first memory blocks; and
7	a column decoder to access data stored in the row cache in response to a column
8	address,
9	wherein the row cache is capable of receiving and storing the entire row of data
10	from the first memory blocks absent the column address.
1	29. (New): The synchronous memory of claim 28 further comprising a
2	plurality of second memory blocks and a second row decoder to access a row of data in the
3 .	second memory blocks in response to a row address, the row cache and the column decoder
4	being disposed between the first memory blocks and the second memory blocks.
1	30. (New): The synchronous memory of claim 28 wherein at least some of
2.	the first memory blocks are paired off to define pairs of memory blocks, the synchronous
3	memory further comprising a plurality of first sense amplifier sets, each pair of memory blocks
4	being associated with one the first sense amplifier sets.
1	31. (New): The synchronous memory of claim 30 wherein at least some of
2	the second memory blocks are paired off to define pairs of memory blocks, the synchronous
3	memory further comprising a plurality of second sense amplifier sets, each pair of memory
4	blocks among the second memory blocks being associated with one the second sense amplifier
5	sets.
1	32. (New): The synchronous memory of claim 28 further comprising means
2	for performing a first precharging operation prior to receiving said "bank activate" command.

1	33. (New): The synchronous memory of claim 28 further comprising means
2	for performing a second precharging operation after said "bank activate" command and prior to
. 3	said "read" command.
1 .	34. (New): An SDRAM comprising the synchronous memory of claim 28.
1	35. (New): The SDRAM of claim 34 wherein the row decoder is capable of
2	accessing a row among the first memory blocks in response to a "bank activate" command.
1	36. (New): The SDRAM of claim 34 wherein the column decoder is capable
2	of accessing data in the row cache in response to a "read" command.
1	37. (New): The SDRAM of claim 34 further comprising an output to which
2	data read from the row cache is moved, the data being moved to the output of the SDRAM a
3	predetermined number of clock cycles after the "read" command.
1	38. (New): The SDRAM of claim 37 wherein the predetermined number of
1 2	38. (New): The SDRAM of claim 37 wherein the predetermined number of clock cycles comprises two clock cycles.
2	clock cycles comprises two clock cycles.
2 ·	clock cycles comprises two clock cycles. 39. (New): A memory device comprising:
1 2	clock cycles comprises two clock cycles. 39. (New): A memory device comprising: first memory blocks;
2 1 2 3	clock cycles comprises two clock cycles. 39. (New): A memory device comprising: first memory blocks; second memory blocks;
1 2 3 4	clock cycles comprises two clock cycles. 39. (New): A memory device comprising: first memory blocks; second memory blocks; a cache disposed between the first memory blocks and the second memory blocks.
2 · · · · · · · · · · · · · · · · · · ·	clock cycles comprises two clock cycles. 39. (New): A memory device comprising: first memory blocks; second memory blocks; a cache disposed between the first memory blocks and the second memory blocks the cache configured to latch a selected row of data read out from the first memory blocks and a
1 2 3 4 5	clock cycles comprises two clock cycles. 39. (New): A memory device comprising: first memory blocks; second memory blocks; a cache disposed between the first memory blocks and the second memory blocks the cache configured to latch a selected row of data read out from the first memory blocks and a selected row of data read out from the second memory blocks; and
1 2 3 4 5 6 7	clock cycles comprises two clock cycles. 39. (New): A memory device comprising: first memory blocks; second memory blocks; a cache disposed between the first memory blocks and the second memory blocks the cache configured to latch a selected row of data read out from the first memory blocks and a selected row of data read out from the second memory blocks; and data buses coupling the selected row of data read out from the first memory

- 1 40. (New): The memory device of claim 39 further comprising a first row 2 decoder to access a row of data from the first memory blocks and a second row decoder to access 3 a row of data from the second memory blocks.
- 1 41. (New): The memory device of claim 40 further comprising a column 2 decoder to access selected data stored in the cache in response to a column address.
- 1 42. (New): The memory device of claim 39 wherein the cache is capable of 2 latching an entire selected row of data from the first memory blocks and latching an entire 3 selected row of data from the second memory blocks.